ABSTRACT

A vertical JFET 1a according to the present invention has an n^+ type drain semiconductor portion 2, an n-type drift semiconductor portion 3, a p^+ type gate semiconductor portion 4, an n-type channel semiconductor portion 5, an n^+ type source semiconductor portion 7, and a p^+ type gate semiconductor portion 8. The n-type drift semiconductor portion 3 is placed on a principal surface of the n^+ type drain semiconductor portion 2 and has first to fourth regions 3a to 3d extending in a direction intersecting with the principal surface. The p^+ type gate semiconductor portion 4 is placed on the first to third regions 3a to 3c of the n-type drift semiconductor portion 3. The n-type channel semiconductor portion 5 is placed along the p^+ type gate semiconductor portion 4 and is electrically connected to the fourth region 3d of the n-type drift semiconductor portion 3.